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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,887	02/02/2004	William A. McGee	TT5556	1070

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THE CAVANAGH LAW FIRM
VIAD CORPORATE CENTER
1850 NORTH CENTRAL AVENUE, SUITE 2400
PHOENIX, AZ 85004

EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/770,887	MCGEE ET AL.	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *21-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-14 and 20* is/are rejected.

7)☒ Claim(s) *4-6 and 15-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2-2-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the election filed May 2, 2005.

Election/Restrictions

Applicant's election without traverse of claims 1-20 in the reply filed on May 2, 2005 is acknowledged.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

Claim 13 recites the limitation "**the first transistor area**" in lines 1-2 on page 19. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3 and 7-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Saito et al. (US 2002/0141232 A1).

In regard to claim 1, Saito et al. teach a memory element comprising a memory cell MJT having an aspect ratio less than one (1:2), wherein the aspect ratio is a ratio of a first dimension of the memory cell to a second dimension of the memory cell, the first dimension in the direction of a bit line BL of the memory element and the second dimension in the direction of a word line WL of the memory element (Figure 19, page 1, paragraph [0023]).

In regard to claim 3, Saito et al. teach a 6T memory cell (Figure 18).

In regard to claim 7, Saito et al. teach a semiconductor substrate having a major surface; and a first metallization system disposed over the major surface, wherein the pair of bit lines BL comprise a portion of the first metallization system (Figures 18-19).

In regard to claim 8, Saito et al. teach a second metallization system over the first metallization system, wherein the word line WL comprises a portion of the second metallization system (Figures 18-19).

In regard to claim 9, Saito et al. teach a first shielding element (left) 204 adjacent one side of the word line WL 203 (Figures 11 and 18-19, page 8, paragraph [0140]).

In regard to claim 10, Saito et al. teach a second shielding element (right) 204 adjacent an opposing side if the word line WL 203 (Figures 11 and 18-19, page 8, paragraph [0140]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (US 2002/0141232 A1) as applied to claims 1, 3 and 7-10 above, and further in view of Kawakubo et al. (US 6,165,837).

Saito et al. teach all mentioned in the rejection above.

However, Saito et al. fail to teach an aspect ratio less than 0.5.

Kawakubo et al. teach an aspect ratio of 1 or less (column 3, lines 4-7) which fits in the range of less than 0.5 .

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the memory element structure as taught by Saito et al. with the memory element having an aspect ratio less than 0.5 as taught by Kawakubo et al. to provide a memory device which can attain high integration density and high process yield (column 2, lines 45-48).

Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ema (4,975,753) in view of Tottori (US 6,265,778).

In regard to claim 11, Ema teaches a memory element, comprising: a substrate 11 having a major surface; a memory cell formed from the substrate 11, the memory

cell including at least one silicided portion 22_1; a first layer 23 of dielectric material disposed over the major surface and the at least one silicided portion 22_1; a bit line metallization system 30_1; and a word line metallization system disposed 24_1, 24_2 and 24_3 over the bit line metallization system 30_1 (Figure 2, columns 3-4, lines 54-68 and 1-48, respectively).

However, Ema fails to teach a bit line metallization system disposed over the first layer of dielectric material.

Tottori teaches a bit line metallization system 11 disposed over the first layer 61 of dielectric material (Figures 1 and 8, column 5, lines 13-22).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the memory element structure as taught by Ema with the memory element having a bit line metallization system disposed over the first layer of dielectric material as taught by Tottori to enhance device integration (abstract).

In regard to claim 12, Tottori further teaches a 6T memory cell (Figure 1).

As best understood and in regard to claim 13, Tottori teaches a first doped region 413 of a first conductivity type, the first doped region having a first pass transistor area 6a and a first driver area 6b; a second doped region (well region) of a second conductivity type, the second doped region (well region) abutting the first doped region 413; a first gate structure 412 having first and second sides disposed over the first transistor area, wherein a first portion of the first pass transistor area 6a adjacent the first side of the first gate structure 412 is coupled to a first bit line 11; and a second gate

structure 412 having first and second sides disposed over the first driver area 6b and over the second doped region (well region), wherein a portion of the first driver area 6b adjacent the first side of the second gate structure 412 is between the first side of the second gate structure 412 and the second side of the first gate structure 412 and wherein a portion of the first driver area 6b adjacent the second side of the second gate structure 412 is coupled for receiving a first source of operating potential (at 24) (Figures 1 and 8, columns 5 and 8, lines 13-22and 1-13, respectively).

In regard to claim 14, Tottori teaches the first and second gate structures 412 being substantially parallel to each other (Figures 1 and 8).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ema (4,975,753) and Tottori (US 6,265,778) as applied to claims 11-14 above, and further in view of Fujiwara (US 6,674,120 B2).

Ema and Tottori teach all mentioned in the rejection above.

However, Ema and Tottori fail to teach a silicon-on-insulator substrate.

Fujiwara teaches a silicon-on-insulator substrate (Figure 32, column 29, lines 1-26).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the memory element structure as taught by Ema and the memory element having a bit line metallization system disposed over the first layer of dielectric material as taught by Tottori with the memory element having a

silicon-on-insulator substrate as taught by Fujiwara to improve electrical performance (column 29, lines 58-62).

Allowable Subject Matter

Claims 4-6 and 15-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to memory elements:

Goebel et al. (US 6,309,930 B1)

Kimura (5,359,206)

Li et al. (US 6,184,103 B1)

Narui et al. (US 6,635,918 B1)

Sivan (5,198,683).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
June 23, 2005